**PREDICATED EXECUTION OF INSTRUCTIONS IN PROCESSORS**

[ABSTRACT OF THE DISCLOSURE]

A processor, operable to execute instructions on a predicated basis, includes a series of predicate registers (135), a control information holding unit (131) and a plurality of operating units (133). Each predicate register of the series (135) is switchable between at least respective first and second states and each is assignable to one or more predicated-execution instructions. The control information holding unit (131) holds items of control information which correspond respectively to the predicate registers, and each operating unit also corresponds individually to one of the predicate registers. Each operating unit has a first control input connected to the control information holding unit (131) for receiving the control-information item corresponding to its unit's own corresponding predicate register and also has a second control input connected for receiving the control-information item corresponding to a further one of the predicate registers. Each operating unit is operable to perform one or more state determining operations in which the state of its own predicate register is determined in dependence upon the received control-information items. In one embodiment, the operating units are operable in parallel with one another to perform respective such state determining operations. The state determining operations can be used to bring about state changes required in prologue, kernel and epilogue stages of a software-pipelined loop.

[Fig. 12]